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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

03103837.5

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

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If no title is shown please refer to the description.
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Power Saving by Disabling Cyclic Bitline Precharge

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D E S C R I P T I O N

Power Saving by Disabling Cyclic Bitline Precharge

1. BACKGROUND OF THE INVENTION

1.1. FIELD OF THE INVENTION

The present invention relates to computer hardware and in particular to power management of high frequency storage designs which are able to implement differential write or read access in a dynamic hardware arrangement of storage cells having some inner segmentation. More particularly, the present invention relates to a method and respective system of accessing memory cells within a dynamic hardware memory block operated with a precharge mechanism, in which differential read/ write accesses are performed by activating true and complement bit lines.

1.2. DESCRIPTION AND DISADVANTAGES OF PRIOR ART

Basically, there is a strong need for power saving in computer systems. This need is in particular very significant in handheld devices or notebook computers in applications or situations in which the device is not connected to a mains supply voltage. It is known to realize power saving by switching OFF or switching ON STANDBY predetermined parts of the computer device, when the user does not perform any user action on the device, e.g. pressing a key or moving a mouse pointer, etc.

A second, important type of power saving is implemented, however, during the operation of the device. The present invention concentrates to the latter one.

In modern storage array designs several storage cells are connected to one write-head and one read-head in form of a sense

amplifier via pairs of bitlines, abbreviated herein as BL, whereby each pair of bitlines consists of one "true" and one "complement" bitline. For fast access time and low power consumption the bitlines are precharged according to prior art technology each cycle to read data from and write data to the cells. A separate signal input controls if data is written or read. It is a specific feature of so-called differential write and read access implemented by a pair of bitlines to read from or write to a memory cell, or an entire segment comprising a sub-array of memory cells, that in any write access one bitline must be drawn to high and the other must be drawn to zero independently of the bit value to be written.

With special reference to the aspect of power saving during operation it should be noted that prior art differential writing entails a complete discharge of one bitline of the regarded bitline pair. This is depicted in **fig. 1**, where a bitline TRUE denoted there as BLT, is drawn to lowlevel at time t = t1, t3 or bitline COMPLEMENT denoted there as BLC, is drawn to lowlevel at time t = t5, t7 and so on. By way of contrast, reading discharges the bitline only partly, see bitline COMPLEMENT BLC at t = t8. Directly after the data is written or read, the bitlines are usually precharged for the following cycle in a so-called restore process, in fig. 1 at time t = t2, t4, t6, t9 and so on.

The prior art precharging techniques count for a significant amount of array power since an array comprises a large number of bitlines and each of them is relatively long. The power consumption for a read cycle is lower than for a write cycle because the bitlines are not totally discharged in the read cycle case. It should be noted, however, that complementary system hardware like power supply or test equipment must be designed for peak array power during the write case. As the total chip power is typically composed of clock power (40 %), array power (40 %) and power for logic (20 %) the skilled reader

understands that power saving for the array power may have a chance to reduce the total power significantly.

The US patent no. 5,848,015 to Sony Corporation discloses a specific technique for reducing the power consumed during sequential read accesses of the memory cells within a memory block. According to this prior art approach power saving is limited because it is first restricted to read accesses and does not include write accesses, and second this technique basically moves the time at which precharging takes place to a later time, namely when the memory access to the last memory cell within a given row is complete. Thus, this method can only be applied in particular application cases in which a sequential read of the memory cells within one and the same row of a given memory block takes place extending over several cycles. In the general case, however, in which the access is non-sequential, cycle-selective and directed to a complete segment of an array - as it is the case with the most state of the art memory cells - this prior art method can not be efficiently applied. Further, this prior art disclosure leaves out the possibility to save power during write operations.

1.3. OBJECTIVES OF THE INVENTION

It is an objective of the present invention to provide an improved method of accessing memory cells within a memory block, which reduces power consumption.

2. SUMMARY AND ADVANTAGES OF THE INVENTION

This objective of the invention is achieved by the features stated in enclosed independent claims. Further advantageous arrangements and embodiments of the invention are set forth in the respective subclaims. Reference should now be made to the appended claims.

The basic approach of the present invention comprises the idea to

a) determining whether or not an access following to a current one will be a read or write access, and

b) performing a precharge of bitlines only in case of a following read access.

This can be realized for example by activating a "precharge" signal in order to restrict precharging to be performed only in those cases, in which it is determined that precharging is really needed, namely when the next following access to said memory block will be a read access. When a write access follows, that signal would be deactivated and precharging is avoided. By that, the knowledge is exploited that reading using a sense amplifier requires precharged bitlines, whereas precharging is not necessary for writing.

Thus, according to the invention a conventional precharge control signal may be combined with an external control signal telling if the next cycle is a read cycle. If the combination is for example a simple AND-logic, then a new effective precharge signal is generated that permits precharging of bitlines, when those bitlines are used for a write access in a respective next cycle. Thus, when the new precharge signal generated according to the invention is exploited at the end of a current cycle n, for example in a restore phase of this cycle n, a respective bitline will not be precharged when the new precharge control signal tells that in the following cycle n+1 data will be written to the respective memory segment.

The advantage results that, when a bitline carries a logical 1 (BL "true" is charged, BL "complement" is discharged) at cycle n, and a logical 1 value shall be written at cycle n+1 to a cell that is connected to the same pair of bitlines, then the power of precharge can be saved.

The power saving is complicated to calculate precisely from a theoretical point of view. It will be quantifiable more reliably by test runs of an inventional chip. Thus by now, the power saving is estimated to be in a range between 5% and 10%, when a statistically balanced read/write distribution is assumed.

Beyond that power saving a secondary advantageous effect can be mentioned that complementary hardware that has to meet peak power requirements, can now be designed for a lower peak power level, as peak power is significantly defined by the power needed during those precharging before write cycles in prior art.

The invention can be advantageously applied for SRAM arrays.

3. BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and is not limited by the shape of the figures of the drawings in which:

Fig. 1 is a voltage over time diagram illustrating the discharge and precharge of bitlines in prior art for a write and a read access, and illustrating in broken lines the avoiding of precharging according to the invention;

Fig. 2 is a schematic block diagram representation illustrating the basic inventive idea to combine an existing external signal "read cycle n+1" and a "conventional precharge signal" in an AND-gate and thus generating a new precharge signal for a respective array segment; and

Fig. 3 is a schematic block diagram representation illustrating the use of the external control signal "read cycle n+1" in fig. 2.

4. DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

As it reveals from **fig. 2** the above-mentioned external signal 22 "read cycle n+1" is ANDed in an AND-gate with the conventional precharge signal 20 and thus leading to an effective precharge control signal 24, which may be used for controlling a respective memory segment. Of course, the combination of the two signals 20 and 22 to generate the effective precharge signal 24 is not restricted to an AND-gate, but can be also achieved by other gates.

With reference back to fig. 1 attention is drawn to the broken lines in the bitline TRUE BLT diagram and in the bitline COMPLEMENT BLC diagram, which show the benefit achieved by the present invention. The benefits are twofold, namely, that the bitlines are not precharged when a write access follows after a write access -see broken line A and B in the BLT and BLC-signal, and that the bitlines are not precharged when a write access follows after a read access -see broken line C. However, benefits can only be achieved when the data, associated with that specific bitlines does not change its value from cycle n to cycle n+1. Thus, no savings between t4 and t5 are achievable).

Next, three examples how to get the above-mentioned external signal "read cycle n+1" will be introduced next below:

1. read/write given by array function

In some cases the read/write information is given inherently by the function of the memory array. For example in an applicational case first, all data is completely written to the array, and later, data is only read without further writing. Thus, in cases in which the write accesses are done over a longer period of time, as it is known and required by a

respective application, the "read cycle n+1" signal may be set to "1" for the whole writing period.

2. read/write is known two system cycles in advance

This situation is depicted in **fig. 3**, in which cycles increase from left to right and the progress is illustrated to develop from top to down. In this example there is any time consuming overhead depicted with reference sign 31, the doing of which requires some time, which may be used to make the before-mentioned external signal "read cycle n+1" available for generating the new precharge signal according to fig. 2. In this case the read/write signal is available basically two system cycles in advance. When for example generating the array address takes two or more cycles, then the before-mentioned "read cycle n+1" signal is available at the right time.

3. no operation (no op)

When none of the above methods is applicable it is possible according to a preferred aspect of the present invention to generate the required overhead expressedly with a no op cycle. This case is to handle in an analogous way to the situation depicted in fig. 3, in which "overhead" is replaced by "no op". The nominal drawback of the delay of one cycle at each start of the array can be tolerated in many cases due to the considerable powersaving and due to the fact that during operation data is returned each cycle, nevertheless.

C L A I M S

1. A method for accessing memory cells within a dynamic hardware memory block operated with a precharge mechanism, in which differential read write accesses are performed by activating true and complement bit lines characterized by the steps of:

a) determining whether or not an access following to a current one will be a read access, and
b) performing a precharge of bitlines only in case of a following read access.

2. The method according to claim 1, in which an SRAM array comprises said memory cells.

3. The method according to claim 1, in which a precharge control signal (20) is combined together with a control signal (22) evaluating, if a next cycle comprises a read access or a write access.

4. The method according to the preceding claim, in which said control signals (20, 22) are combined to yield an effective precharge signal (24).

5. A computer chip comprising memory cells operated according to the method of claim 1 to claim 4.

6. The computer chip according to claim 5 comprising means for combining a precharge control signal with an external control signal telling if the next cycle is a read cycle.

7. The computer chip according to claim 6 in which said means for combining is an AND-logic.

8. An SRAM chip according to the preceding claim.

9. A computer system having a chip according to the preceding claim.

A B S T R A C T

The present invention relates to computer hardware and in particular to power management of high frequency storage designs, which are able to implement differential write or read access in a dynamic hardware arrangement of storage cells having some inner segmentation. More particularly, the present invention relates to a method and respective system of accessing memory cells within a dynamic hardware memory block operated with a precharge mechanism, in which differential read/ write accesses are performed by activating complementary bit lines. In order to decrease power consumption, it is disclosed to perform the steps of:

a) determining whether an access following to a current one will be a read or a write access, and

b) performing a precharge of bitlines only in case of a following read access.

According to the invention a conventional precharge control signal (20) may be combined with an external control signal (22) telling if the next cycle is a read cycle. The combination of the two signals can be used, for example, as input to a simple AND-logic to generate an effective precharge signal (24). This signal permits precharging of bitlines only when those bitlines are used for read access in a respective next cycle.

(Fig. 2)

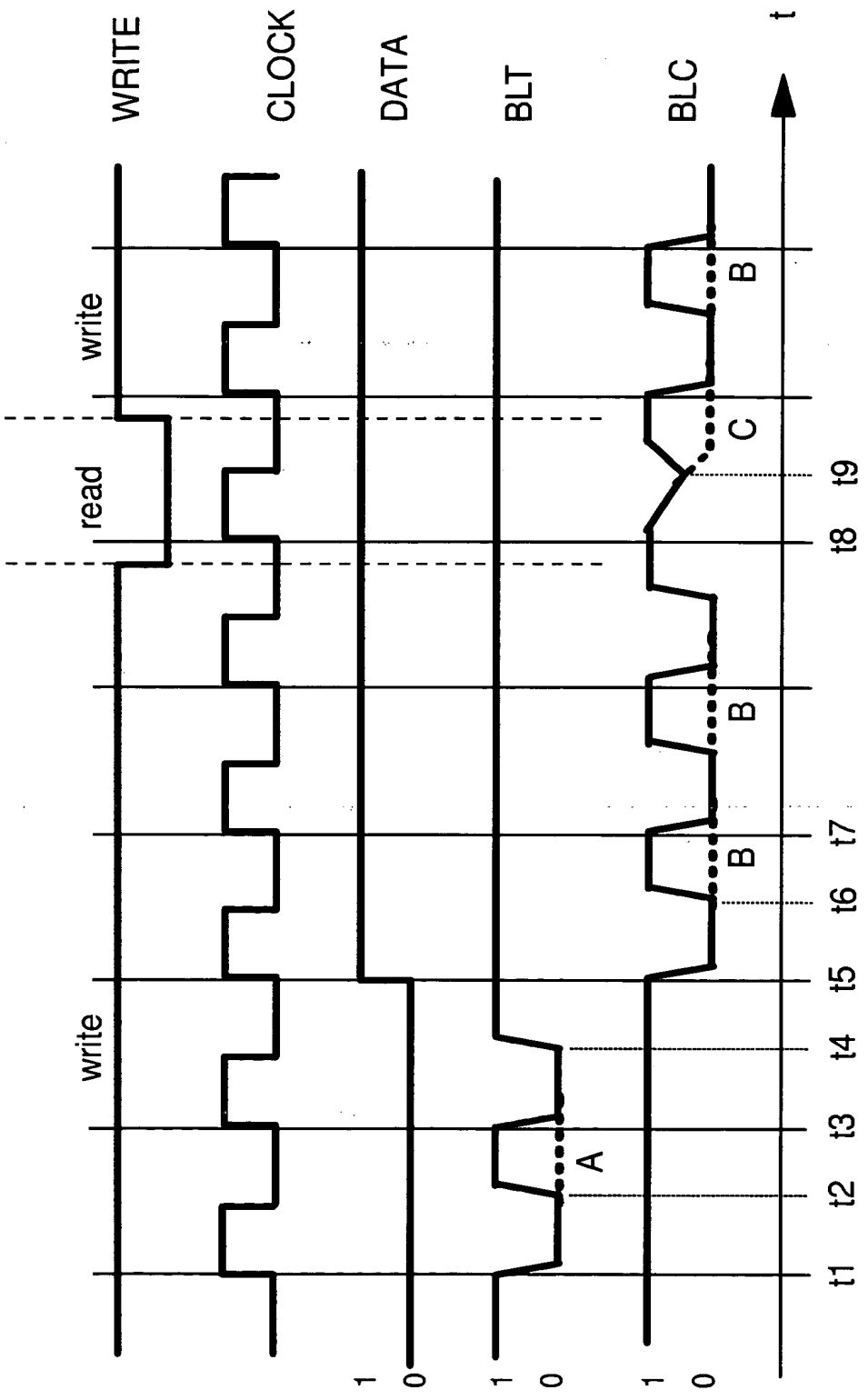
WRITE
CLOCK
DATA
BLT
BLC
t
write
read
write
A
B
B
B
C
B
t1
t2
t3
t4
t5
t6
t7
t8
t9
1
0
1
0
1
0

FIG. 1

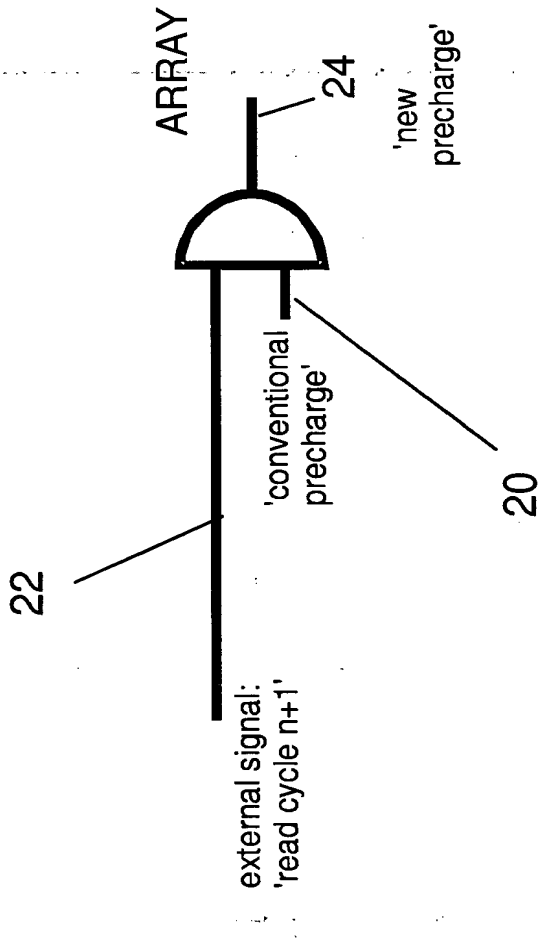
ARRAY
24
'new precharge'
'conventional precharge'
20
22
external signal: 'read cycle n+1'

FIG. 2

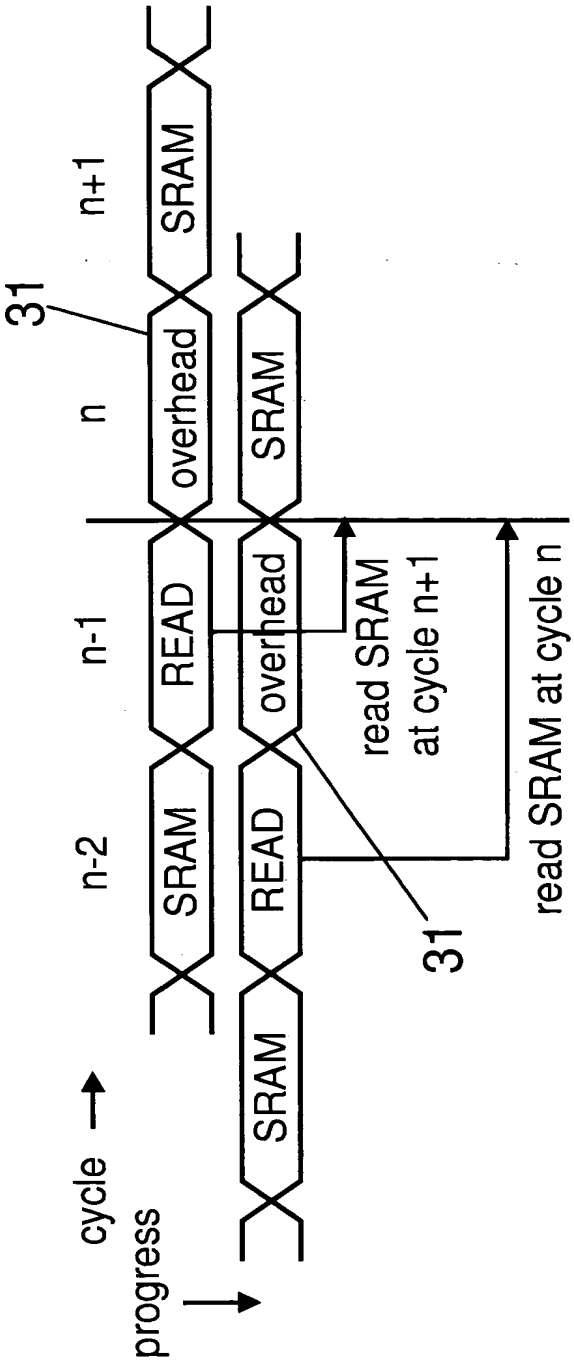
n-2
n-1
n
n+1
SRAM
READ
overhead
SRAM
SRAM
READ
overhead
SRAM
31
31
read SRAM
at cycle n+1
read SRAM at cycle n
cycle
progress

FIG. 3